POTENTIAL INDUCED DEGRADATION OF SOLAR CELLS AND PANELS

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ABSTRACT

Since solar energy generation is getting more and more important worldwide PV systems and solar parks are becoming larger consisting of an increasing number of solar panels being serially interconnected. As a consequence panels are frequently exposed to high relative potentials towards ground causing High Voltage Stress (HVS). The effect of HVS on long term stability of solar panels depending on the leakage current between solar cells and ground has been first addressed by NREL in 2005 [1]. This potential degradation mechanism is not monitored by the typical PV tests listed in IEC 61215 [2].
Depending on the technology different types of Potential Induced Degradation (PID) occur. This paper is focusing on PID of wafer based standard p-type silicon technology aiming on increasing life times for solar panels once exposed to external potentials in the field. A test setup is presented for simulation of the PID in the lab and the influence of cell properties on PID is demonstrated in order to reveal the cell being the precondition for the PID. However, PID can also be stopped or minimized on panel and system level as shown in the paper.

BACKGROUND

The most prominent case for PID in silicon solar cell technology is Sunpower's polarization effect [4] but also other technologies like a-Si and ribbon silicon have been reported in the past to be prone to different types of PID under certain circumstances– either reversible e.g. polarization or irreversible e.g. electro chemical corrosion [3]. All known PID effects have one common characteristic the degradation is depending on the polarity and level/extent of the potential between cell and ground. Different standards exist concerning the configuration of a PV system. E.g. in Europe system voltages up to 1000V and for the US only up to 600V are allowed. Some countries dictate or recommend PV system grounding configurations others do not. Accordingly, inverters technologies without transformer are commonly used in Europe whereas in the US it is not common to use transformer less inverters since PV systems are usually grounded.
It is the combination of several parameters such as high potential towards ground and a PID prone solar cell embedded in a standard panel configuration which can cause significant power degradation in the field within a panel's life time. So the reduction of the PID of standard H-pattern cells – first identified in 2009 – is a clear track for life time extension of a solar panel and for the reduction of the overall degradation of a panel after a certain amount of time.

To better understand the cause of PID three different levels – system, panel and cell – are separately investigated.

System level

On system level the potential difference between ground and cell is the most important factor for PID. The system voltage depends in first order on the number of panels serially interconnected and the irradiation and in second order on the panel temperature. Depending on the configuration of the grounding the potential of a cell towards ground is negative or positive. Three different possibilities exist – two of these are to ground one of the system poles (PV-/PV+ grounding) then all cells/panels are positive or negative towards ground or if no pole is grounded the resulting potential is not fixed for which reason it is called floating potential. In the latter case one part of the string has a negative and the other a positive potential towards ground.

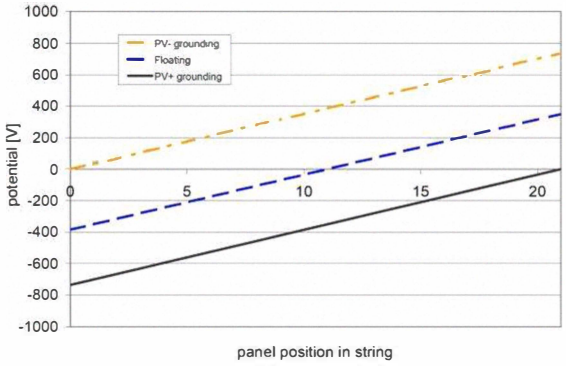

Figure 1 String potential, three grounding schemes PV+/PV- and no grounding (floating potential).

Panel level

Environmental factors such as humidity and temperature influence leakage currents between ground and cell [1].

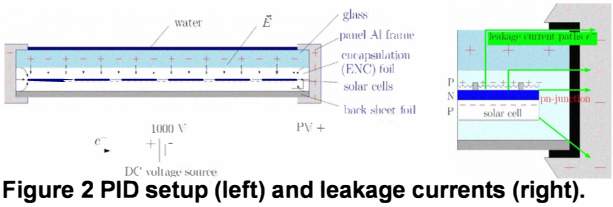

Figure 2 PID setup (left) and leakage currents (right).

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If water penetrates the solar panel the leakage current rises due increasing conductivity of the encapsulation (ENC) material.
The interaction of ENC material, back sheet foil, glass, and frame is resulting in certain leakage current paths as illustrated in figure 2. Additionally material properties production processes and panel layout do play a role for the HV-durability of panels.

Cell level

On cell level some process steps as well as the quality of the base material have been identified to significantly contribute to the extent of PID tendency on cell level. In the result chapter we take a closer look at the different parameters that influence the PID.

EXPERIMENTAL

For characterization of the cells and panels prior and after the PID test a flash tester and a high resolution electroluminescence (EL) camera is used.
A PID setup was built to test coupons (single cell laminates) or standard panels consisting of sixty cells. The glass on the sunny side is flooded with water or covered with a wet blanket.
This conductive front cover is connected to the positive pole and the panel contacts are connected to the negative pole of a power supply in order to generate a typical bias voltage of 1000V (maximum system voltage in Europe) for standard p-type solar cells. Choosing the setup described above a negative cell voltage versus ground – as occurring in the field - is simulated. A standard test is taking 100 hours and afterwards the samples are retested and the results are compared to the initial measurements.
To investigate the leakage currents from cell to ground an ampere meter with data logger was used. In order to evaluate the impact of environmental factors such as temperature and humidity on the test – panels were placed in an environmental chamber under defined conditions.

EXPERIMENTAL RESULTS

System level

The following example (fig.3) shows an EL image of a floating system that is affected by PID. The arrow indicates the rising system voltage. When going from negative potential (left) to positive potential (right) versus ground. Degradation stops when the potential turns from negative to positive.

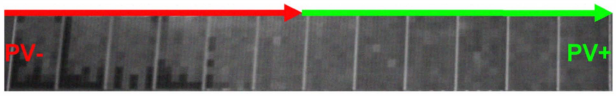

Figure 3 EL image of a floating PID string with degraded panels on the side with negative potential.

In case the potential is not floating but fixed in the way that the PV- pole of the string is grounded PID can be effectively prevented.

However, in the last years inverter development was resulting in higher efficient technologies partly due to the abandonment of transformers. As a consequence grounding is not possible and PID has to be prevented with another approach.

Panel level

Taking a closer look at the PID effect on the panel level as done in case of prone solar cells in a standard panel – see the following EL images before and after the PID test with 1000V for 100hr. First in general the brightness of the picture is decreasing (not visible here) and second single cells are not uniformly affected. Some cells degrade heavily and seem to be short circuited while others appear to be stable. The reasons for this variation must be investigated on cell level as will be done in the next chapter.

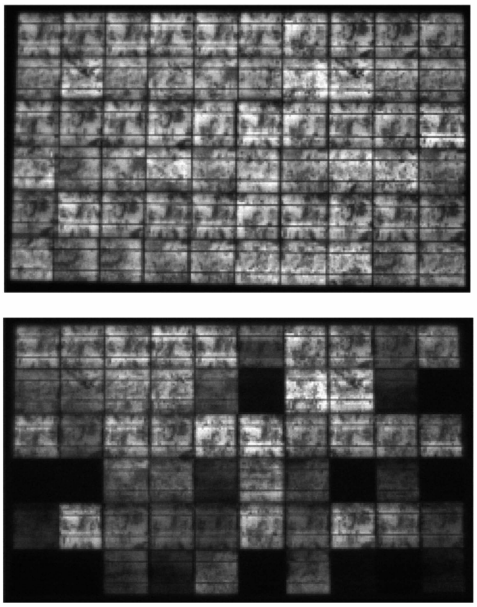

Figure 4 EL image of a panel before (upper) and after (lower) 100hr 1000V PID test – power loss was 32%.

The influence of the material composition in the panel was tested systematically with solar cells that are prone to PID. A crosscheck with non sensitive cells showed no PID for all material combinations. In the material comparison it turned out that an important factor to reduce PID in case of prone solar cells is the type of ENC material. In the following figure is shown the leakage current at 1000V as a function of time during a temperature ramp up from -20℃ to 48℃ in a humid atmosphere (50% RH). It can be seen that two different ENC materials are causing the peak leakage currents to differ by more than one order of magnitude. The panel can be described here as a

capacitor being charged while the temperature is rising. Finally the full capacity is reached and the current drops.

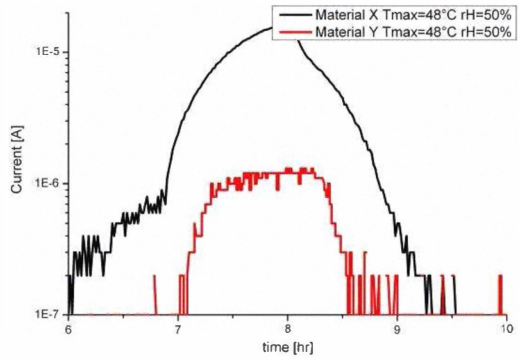

Figure 5 Leakage current for two panels with different ENC material during a temperature ramp from -20℃ t o 48℃ with 1000V applied voltage (RH 50%).

As a consequence of this significant difference in leakage current the PID results with varying ENC materials differs strongly as shown below for three materials in combination with prone solar cells.

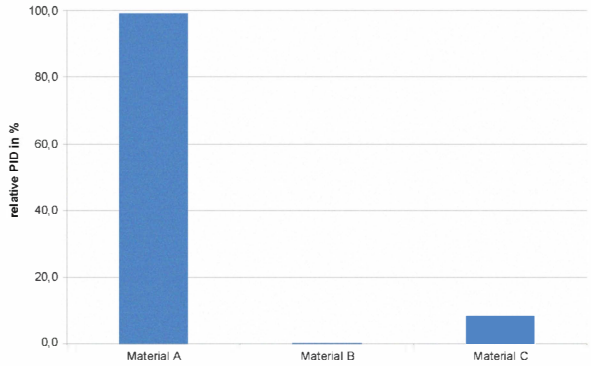

Figure 6 PID comparison of three different ENC materials in panels with prone solar cells.

In order to minimize or avoid PID on panel level and therefore to increase life time and reliability the appropriate material combination have to be found making sure that solar cells prone to PID are combined with ENC materials resulting in low leakage currents on panel level. There are alternative materials to standard EVA better performing in respect to PID but other criteria like price, handling, long term stability issues and availability have to be taken into account.
So although it was shown that it is possible to suppress PID in case of prone cells by switching the ENC material it seems to be even more favorable to minimize or avoid PID on cell level which is discussed in the following chapter.

Cell level

The following two graphs show the evolution of the IV curve with ongoing PID and the corresponding power degradation over time.

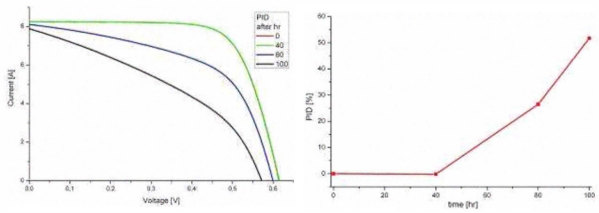

Figure 7 PID IV curve evolution (left) and corresponding power degradation (right).

In case of PID shunt resistance as well as the reverse bias current is affected first followed by FF. Finally Voc decreases reflecting the junction to be less capable of separating holes and electrons.

Time	Uoc	Isc	P	FF	I(-12V)	Rsh
[hr]	[V]	[A]	[W]	%	[A]	[Ω]
0	0,615	8,240	3,616	71,4	0,21	80,4
40	0,615	8,258	3,622	71,3	0,30	51,1
80	0,600	8,109	2,658	54,6	>10	0,5
100	0,572	7,882	1,746	38,7	>10	0,2
rel. PID	-7%	-4%	-52%	-46%	-	-100%

Table 1 Cell IV key parameter change during PID.

The Isc is the parameter that is least affected but with advancing PID Isc also degrades. Depending on the degree of PID the junction is loosing its blocking characteristic under reverse bias or totally breaks down (ohmic shunt). This phenomenon can be visualized by EL images taken during a PID test that are shown in the upper row. After 40hr local shunts appear along the edge of the cell that degrade further from diode to ohmic behavior, as can be seen in the reverse bias image in the lower row. First shunted areas appear bright but after further PID evolution these areas do not emit any more breakdown light [6]. Finally after 100hr both images are dark because of dominating ohmic shunts.

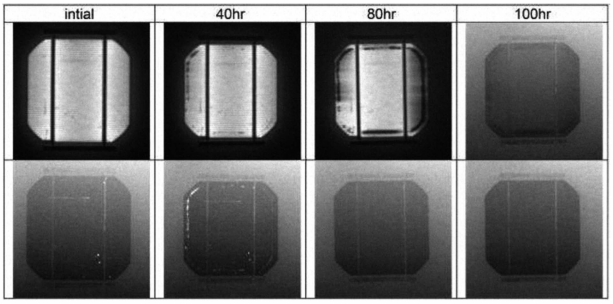

Figure 8 EL image of a cell during PID test (upper row) and reverse bias (-12V) image (lower row).

The leakage current in form of electrons or ions is resulting in an increased charge concentration above the solar cell in the ENC. These charges interact with the emitter and depletion layer and disrupt their function. From semiconductor industry similar effects are known as (time dependent) dielectric breakdown or surface inversion [5]. The electric field of these charge carriers is influencing the

p-n-junction in that way that junction gets more conductive and the local shunt resistance drops. Sunpower applied a transistor model to the polarization effect [4] on their n-type back contact cell. In the case of standard p-type cells this model also works but the configuration needs to be switched from npn- to pnp-transistor.
There are numerous factors on cell level being important in respect to PID. In the following we present the parameters indentified to have a significant impact.

Wafer material

In joint experiments with different cells suppliers SOLON tested the influence of wafer material properties. The most promising parameter that can be varied here is the base resistivity.

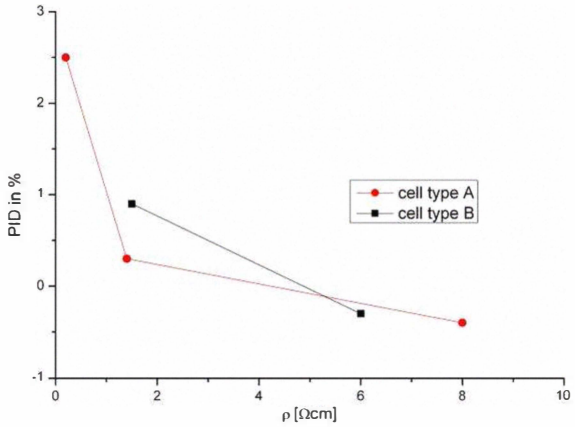

Figure 9 Base resistivity dependence of PID.

In two experiments base doping was varied by almost two orders of magnitude. The result is that increasing the base resistivity leads to more resistant solar cells concerning PID since lower base doping leads to a wider depletion region at the junction when the emitter doping is held constant.

Within different experiments with cell suppliers where cells have been produced at constant cell processing parameters utilizing different wafer suppliers a significant batch dependence has been found. This could hint on systematic variation of certain wafer properties relevant for PID.
Lower quality silicon or comparably high concentrations of crystal defects seem to increase PID but here results have to be further verified.

Emitter diffusion

The cell process typically starts with a cleaning followed by a texturization step – depending on wafer type and process acidic or alkaline textures are applied. Here the results do not show a clear trend. But for example if texturization is incomplete or residues are left on the surface the following process steps can be affected and hence also PID.

In a typical process the emitter diffusion is the following step and an influence was expected and also found during the test.

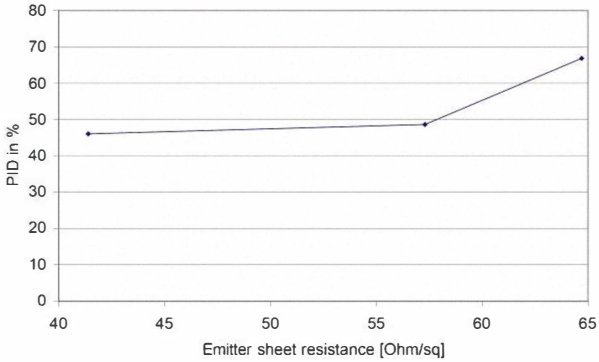

Figure 10 Emitter sheet resistance dependence of PID.

Increasing the emitter sheet resistance leads to a higher sensitivity for degradation of the solar cells.
This trend shows that the cell process optimizations like increasing the emitter sheet resistances as was done in the last years can lead to a higher tendency for PID. Future trends like selective emitter technology must be watched and tested closely. Inhomogeneous emitter diffusion can also play an important role.

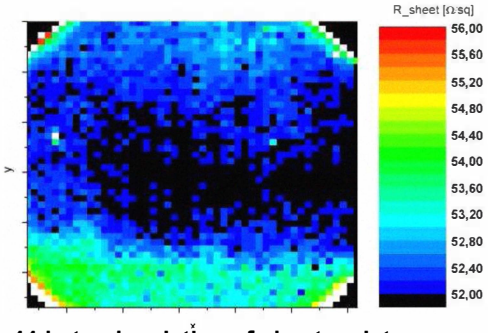

Figure 11 Lateral variation of sheet resistance on a mono crystalline wafer (four point probe).

In the image above the sheet resistance of a mono crystalline wafer (measured with a four point probe after POCL diffusion) is shown. The phases of the wafer show a higher sheet resistance and in general emitter doping is not totally constant over the whole area. Having in mind our findings for the emitter sheet resistance local variations can lead to higher PID sensitivity.

Emitter back etching and edge isolation

Some cell manufactures use emitter back etching methods for edge isolation or for removal of the so called dead layer of the emitter.
Depending on process parameters the sheet resistance can be increased significantly and therefore PID can be increased corresponding to figure 10.

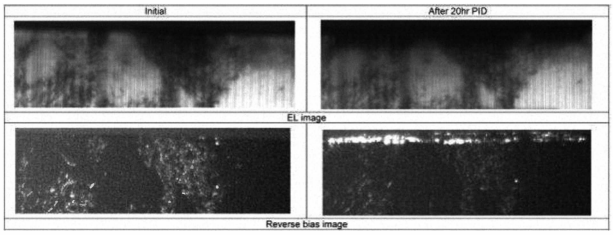

Figure 12 Section of an EL (upper) and reverse bias image (lower) of a cell with chemical etch isolation during PID test (initial and after 20hr).

In figure 12 EL images and reverse bias images at -12V of a solar cell with wet chemical edge isolation before and after a PID test step of 20hr are shown. In the EL image the edge is turning dark while at reverse bias the edge signal is getting more intense explainable by an insufficient edge isolation.
In this case described above edge isolation the emitter was removed not only on the edge but on the surface as well resulting in an emitter with locally high sheet resistance. This example shows that variations in the cell process which are thought to be of no relevance for later application can lead to degradation when the cell is exposed to a potential in the field. Here the PID test reveals potential weaknesses of a solar cell.

Anti-reflective coating

The process step within cell production found most important concerning PID is the anti reflective coating (ARC) deposition. As shown by Sunpower this layer has a significant influence on the PID effect for back contact cells [4]. In case of typical standard cells this layer consists of Si and N, the ratio of these elements, layer thickness and the deposition technique define the character of this layer.
In semiconductor industry a comparable phenomenon is known as dielectric breakdown of passivation layers – but not all properties can be transferred to solar cells [5].

In the graph below the dependence of PID on the Si-N ratio – corresponding to the refractive index (RI) and thereby to the optical characteristics – is shown. PID rates were determined on panel and coupon level.
First result: Si-rich layers tend to show lower degradation than N-rich layers.

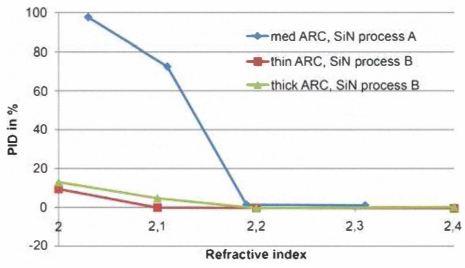

Figure 13 AR-coating: RI, thickness and deposition method dependence of PID.

Besides the RI the layer thickness is important since these two parameters must be well adjusted to reduce reflectivity of the cell. The second result is that a reduction of layer thickness is resulting in lower PID sensitivity (figure 13 thick and thin ARC method B). Going to thinner ARC layers with higher Si/N ratio can be a feasible way of reducing PID.
The third parameter having an impact here is the homogeneity of the resulting SiN layer which is found to be clearly different for various SiN deposition methods – see figure 13 process A&B. However, it can be stated that a homogenous process lowers the risk for PID with standard thickness and RI.

General remark on cell process

Controlling PID at the end of the cell line by special sorting criteria is not possible to our knowledge but adaption of cell processes as well as process control and sensitive wafer material choice allows avoiding PID on cell level.

RECOVERY METHODS

Reverse potential

Provided that electrochemical corrosion is excluded laboratory test with at reverse polarity show that PID is reversible also for standard solar cell similar to what was found by Sunpower for their back contact technology [4].

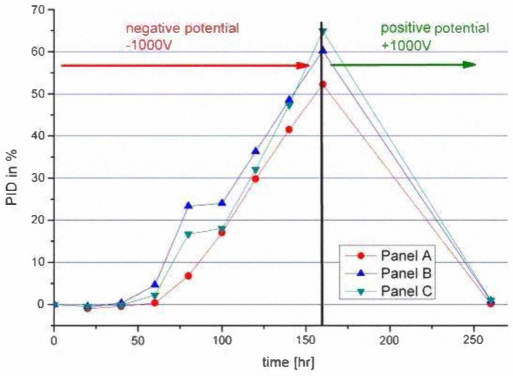

Figure 14 Panel PID and recovery by reverse potential.

As a consequence grounding of the positive pole of the PV system and thereby avoiding of harmful potentials leads to regeneration of affected solar panels. This recovery process takes time and the rate depends on the potential and environmental factors such as humidity and temperature.

Temperature

In the lab a similar behavior was found for the recovery of PID panels by temperature, storing PID panels at around 100℃ for 10 hours lead to a recovery close to 100% but the initial power was not reached after this time step.

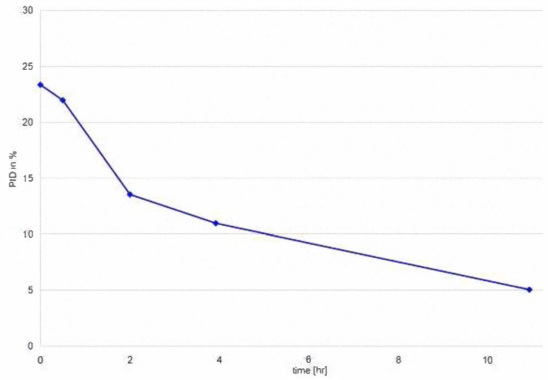

Figure 15 PID recovery by temperature (~100℃).

This test shows that temperature is not only leading to a faster PID evolution (compare figure 5) because of increased leakage currents but it also plays an important role in for regeneration processes in a panel. But this recovery procedure at high temperature is not suitable as standard treatment since high temperature is stressing the panel materials and hence affects the long term stability.
As shown the stability of the defect depends on the temperature. E.g. in [5] a similar semiconductor defect (surface inversion) can be recovered by a high temperature step.
Besides treatment on a hot plate or oven also other sources of heat can at least partly recover the solar cell, e.g. UV treatment, climatic chamber test or applying a reverse or forward bias voltage to the panel's poles.

CONCLUSION

This paper presented a degradation mechanism called Potential Induced Degradation (PID) that is getting more important with growing PV system sizes going along with higher system voltages. It was shown that – although the origin of PID is on cell level – it can be minimized or avoided on all levels – system, panel and cell. The solution on system level is choosing an appropriate grounding scheme of the string poles while on panel level the properties of the encapsulation material determine the height of leakage currents that can in case of prone solar cells lead to PID.
On cell level many parameters influence the PID stability of solar cells. Besides base material resistivity and emitter sheet resistance the most important parameter was found to be the anti-reflective coating since adaption of this layer can avoid the effect of PID.
The PID effect can be reversed by switching the polarity and also high temperatures support regeneration.
Taking these findings into account long term stability of solar panels can be significantly improved by adapting processes on all levels in order to minimize PID and therefore optimize the energy output of the PV system over a 25+ year life time.

OUTLOOK

The scenarios investigated with the laboratory test are simulating worst case conditions with high humidity and constantly high voltage. At SOLON an experiment is going on directly comparing laboratory results with outdoor data at different SOLON test sites (Berlin, Tucson, Carmignano) covering also the impact of different environmental conditions [7].

ACKNOWLEDGEMENT

We would like to thank the cell suppliers for their fruitful discussions and their contribution to this work.

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